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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,836	12/30/2003	Sang-Hee Kang	51876P559	9426

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 09/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,836	KANG, SANG-HEE	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,19 and 20* is/are rejected.

7)☒ Claim(s) *4-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 05/16/2005 has been entered.

2. Claims 1-20 are presented for examination.

Drawings

3. The drawings were received on 05/16/2005. These drawings are Figures 2-9.

Response to Arguments

4. The mess of number of application cause the applicant has been received an improper action.

5. Applicant's request for reconsideration of the last Office action is persuasive and, therefore, the last action is withdrawn.

6. Applicant's arguments filed 09/08/2005 have been fully considered but they are not persuasive.

Applicant argues "Figure 1 of AAPA does not illustrate any device that corresponds to repair address comparator 700 of the claimed invention" is improper. The prior art teach 10_1 is a repair address comparator instead of 700 in Figure 12. The device 10_1 is shown in Figure 2 and Figure 5 with output is HITZ<0> indicated for output AED_FUSE in Figure12 of present invention.

Applicant argues that "AAPA does not teach, disclose or suggest a repair circuit controller in response to a delayed control signal output from the comparator delay modeling block for generating one of a repair address enable signal and a normal address enable signal based on a comparison result of an address comparator" is

improper. As shown in prior art Figure 1 and Figure 9, Figure 9 is a comparator delay modeling block generates enable signals AED1 and AED2 and one of these signals is applied to repair circuit controller as shown in Figure 1, (AED).

As described the applicant's argument is improper. Therefore the last rejection still stands.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

8. Claims 1-3, 19-20 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (AAPA).

Regarding claim 1, AAPA discloses a semiconductor device (Figure1) for comparing an input address with a stored repair address, comprising:

a signal controller (50) for generating control signals including enable signal (Figure1, AE) ;

an address latch unit (40) in response to the control signals for latching the input address;

N number of M-bit address comparators (10), each enabled by the enable signal for comparing the input address with the stored repair address;

a comparator delay modeling block (Figure 9) delaying the enable signal a predetermined time ([0027]) ; and

a repair circuit controller (60) in response to the delayed control signal output from the comparator delay modeling block for generating one of repair address enable signal and a normal address enable signal (Figure1,8,RED_ENABLE, NORMAL_ENABLE) based on a comparison result of an address comparator.

Regarding claims 2-3, AAPA discloses a comparator initialization unit (Figure 1,10) for generating an reset signal to enable and initialize the number of N number of M-bit address comparators, and wherein each of the M-bit address comparators includes a fuse enabling means (Figure 2, 11_1) for receiving the reset signal (Figure2, FUSE_RESET) to output a fuse enabling signal (Figure2, FUSE_ENABLE) in response to whether an enabling fuse included in the fuse enabling means blown out or not; plurality of unit repair address comparing means (11_2) for respectively comparing each bit of the input address which latched the address latching means with each the stored repair address which stored repair address comparing means; signal combination means (Figure 2, 12) for signal address outputting a repair signal (Figure5, HITZ) response to results of the plurality of unit repair comparing means, wherein the signal combination means enabled by the fuse enabling signal.

Regarding claims 19, AAPA discloses a semiconductor device (Figure 1) comparing an input address with a stored repair address, comprising:

a signal controller for generating control signals (50) ;

an address latch unit (40) in response to the control signals for latching the input address;

N number of M-bit address comparators (10), each comparing the input address with the stored repair address;

a comparator delay modeling block (Figure 9) delaying the control signal a predetermined time ([0026]); and

a repair circuit controller (60) in response to the delayed control signal (Figure 1, AED) output from the comparator delay modeling block for generating one of repair address enable signal (Figures 1,8, RED_ENABLE) and a normal address enable signal (Figures1,8, NORMAL_ENABLE) based on a comparison result of an address comparator.

Regarding claim 20, AAPA discloses a comparator initialization unit (Figure 1,20) for generating an enable signal enable initialize an number of N number of M-bit address comparators.

Allowable Subject Matter

9. Claims 4-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 4-18 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Applicant Admitted Prior Art (AAPA), and Hiraki et al. (U.S. Patent

No. 6,449,197), Nakahara et al. (U.S. Patent No. 6,496,431), and others, does not teach the claimed invention having a fuse enabling means includes a first transmission gate for outputting the enabling signal as the fuse enabling signal by turning on when the enable fuse is blown out; and a second transmission gate for outputting the supplied signal between the enable fuse and the second MOS transistor as the fuse enabling signal by turning on when the enable fuse not blown out, wherein the first and the second transmission gates are controlled by output signals from the first and the second inverters.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827

7/21/2006